DENSE CONTENT ADDRESSABLE MEMORY CELL

ABSTRACT OF THE DISCLOSURE

A content addressable memory cell (10) comprises a word line 12, a first bit line (14), and a second bit line (16). A pair of transistors (30-31) is arranged to store bits of data at first and second points (35 and 36). A first transistor (26) is coupled to the word line, the first bit line and the first point. A second transistor (27) is coupled to the word line, the second bit line and the second point. The word line voltage is changed in accordance with process parameters to allow conduction by the first and second transistors to compensate for leakage by the pair of transistors. For example, the first and second transistors may be operated in a triode mode.